FORMATION OF HIGHLY DISLOCATION FREE COMPOUND SEMICONDUCTOR ON A LATTICE MISMATCHED SUBSTRATE

Field of the Invention

[0001] This invention relates generally to the field of semiconductor fabrication, and more particularly to a method of forming a highly dislocation free compound semiconductor on a lattice mismatched substrate, and to the resulting semiconductor structure/device.

Background Art

[0002] Growth of high quality thin films of compound semiconductor on substrates with high lattice and thermal expansion coefficient mismatch with the epitaxial thin film layer, such as III-V nitrides on Si, SiC and sapphire substrates, has shown to be very challenging.

[0003] III-V nitride is a field of intense research due to its wide applications for optoelectronic and electronic devices, such as blue and UV light emitting diodes (LEDs) and Laser diodes (LDs), UV detectors and electronic devices such as bipolar transistors. Compared with the currently used and available devices on the market, nitride devices have marked advantages in several aspects. For example, nitride blue laser can provide at least a 400% increase in data storage density on a CD RAM due to its shorter wavelength than those of red and near infrared lasers. On the other hand, the large bandgap of III-V nitride materials make them good candidates for high power and high temperature transistor applications.

[0004] Currently, one of the main remaining problems of III-V nitride materials is the unacceptable high dislocation density due to large lattice and thermal expansion coefficient mismatch between them and substrates (e.g. 16.09% and 17% between GaN and sapphire, and GaN and Si(111), respectively, the most widely used substrates for III-V nitrides). High dislocation density dramatically degrades the performance and reliability of nitride devices and shortens device lifetime.

[0005] In prior methods, a low temperature $Al_xIn_yGa_{1-x-y}N$ ($0<x, y<1$) buffer layer is used, as described by H. Amano, et al, Appl. Phys. Lett., Vol. 48, 35 (1986) and S. Nakamura, Jpn. J. Appl. Phys Vol. 30, L1705 (1991), which has dramatically improved the III-V nitride epilayer quality in terms of morphology, electrical and optical properties. Other methods such as lateral epitaxial overgrowth (LEO) and Pendeoepitaxy (PE) have also shown success in reducing the dislocation density. However, both the LEO and PE methods require several additional processing steps before a low dislocation epitaxial layer of the material can be obtained. Despite the use of a buffer layer as proposed by Nakamura et al. and Amano et al., the dislocation density in as-grown nitride epilayers is still very high (10^8 to 10^9 cm^{-2}) as diagrammatically illustrated in epilayer 10 on substrate 12 in Fig. 1, which limits nitride device performance and applications.

[0006] To solve this problem, it has been proposed to use a compliant universal (CU) substrate by Lo in US patent 5,294,808 and Hwang et al in US patent 6,406,795. If an epilayer is grown on a very thin substrate, the misfit dislocations (due to both lattice and thermal expansion coefficient mismatch) will propagate into and are contained in the thin CU substrate rather than the epilayer since it is energetically more favorable. An example of a layer 14 of $Al_xIn_yGa_{1-x-y}N$ grown on a Si SOI (Semiconductor On Insulator) substrate 16, is schematically shown in Figure 2, in which the thin Si overlayer 18, above a buried oxide layer 20, serves as a thin free-standing substrate. If the thickness of the Si overlayer is lower than its critical thickness, an ideal CU substrate is achieved and the stress between the overgrown epitaxial $Al_xIn_yGa_{1-x-y}N$ layer and the thin Si overlayer will not exceed the critical value that leads to the generation of dislocations at their interface.

[0007] The advantage of using a CU substrate is that it is universal and different epilayers can be grown on the same CU substrate. However, the disadvantages of this approach for growth of III-V Nitride materials include:

[0008] (1) For $Al_xIn_yGa_{1-x-y}N$ /Si heterostructure the critical thickness of Si is around one monolayer, therefore, no ideal CU substrate can be fabricated in this case. With the typical Si overlayer thickness of about 50 to 200nm, some

dislocations will be generated at the interface some of which will penetrate into the overgrown epilayer 14, as schematically illustrated in Fig. 2.

[0009] (2) The thin Si overlayer on the top of SiO_2 may not give enough guiding force to epitaxial growth of polycrystalline $Al_xIn_yGa_{1-x-y}N$ seeding layer (buffer layer) which leads to a low crystal quality in the buffer layer. A thin Si overlayer does not support epitaxial relationship (lattice structure and orientation) needed in high quality $Al_xIn_yGa_{1-x-y}N$ buffer layer. Quality of the subsequent III-V Nitride layers depend highly on the quality of the seeding (buffer) layer.

[0010] Other techniques have been suggested to reduce dislocation density in a top monocrystalline layer as proposed by Bisaro (US Patent 5141894) by Mantl (US Patent 6464780 B1) and Ramdani (US Patent 6,392,257 B1).

[0011] In these earlier patents, monocrystalline buffer layers have been used. However, growth of a monocrystalline AlInGaN thin buffer layer on Si substrate is highly improbable due to the high lattice and thermal mismatch between the two layers and therefore is not suitable in this application.

[0012] The Bisaro patent further describes an embodiment in which a monomolecular preliminary layer is deposited on a substrate, e.g. silicon. The substrate is then implanted through the preliminary layer to create a highly disturbed or even amorphous zone on the surface of the silicon. It is also mentioned that the preliminary layer can also be a thicker amorphous layer. The preliminary layer is used to stabilize the silicon surface and to protect the silicon in the implantation stage only. It does not play the role of a seeding layer for the following monocrystalline layer growth after ion implantation.

[0013] Further, ion implantation will usually cause significant damage to a monocrystalline layer. In the Bisaro patent, it is not mentioned at all how to keep the buffer layer monocrystalline during ion implantation process. In the Mantl patent, light element (hydrogen) ion implantation with low dose is suggested in order to minimize the damage to the monocrystalline buffer layer, which is feasible, but it is not applicable for

high dose ion implantation as needed for this application. Also in the Mantl approach, the monocrystalline epitaxial layer is not disconnected "mechanically" from its substrate and, therefore there is always stress and dislocations present in the layers if the layer thickness exceeds critical dimension.

[0014] In Ramdani, an amorphous intermediate oxide layer is generated by thermal diffusion of oxygen through the thin monocrystalline oxide/nitride accommodating buffer layer, eventually reacting with the monocrystalline substrate at the interface to create the oxide layer. Thermal diffusion of oxygen at temperatures of 400^0C-600^0C (as suggested by Ramdani in column 8, line 62) through a monocrystalline layer of GaN with a practical thickness of 20nm is a very lengthy procedure.

[0015] Thus, a need persists for a practical and cost effective method for forming a highly dislocation free compound semiconductor such as $Al_x In_y Ga_{1-x-y} N$, on a lattice mismatched substrate.

Summary of the invention

[0016] According to the principles of the present invention, the shortcomings of the prior art are overcome, and a highly dislocation free compound semiconductor can be formed on a lattice mismatched substrate by: depositing a polycrystalline buffer layer on the substrate; creating an amorphous layer at an interface of the substrate and the polycrystalline buffer layer; and depositing a monocrystalline template layer of the compound semiconductor on the buffer layer.

[0017] The method may further include growing an epilayer of the compound semiconductor on the template layer.

[0018] The amorphous layer is preferably created by ion implantation, either through the polycrystalline buffer layer, or by back-side ion implantation through the substrate.

[0019] In a preferred embodiment, the amorphous layer comprises an amorphous oxide layer created by oxygen ion implantation; the polycrystalline buffer layer and the

template layer exhibit homoepitaxy, or are closely lattice matched and/or comprise the same material; and the compound semiconductor comprises a III-V material, such as $Al_xIn_yGa_{1-x-y}N$ ($0<x, y<1$).

[0020] In the present invention, the buffer layer serves as a seed layer for growth of the template layer, which, in turn, supports subsequent growth of compound semiconductor based device structures in an epilayer. The amorphous layer serves to "mechanically" separate the compound semiconductor epilayer and the substrate. This separation will make the compound semiconductor layer "floating" on the substrate and the strain between the epilayer and the substrate will be released, which in principle will lead to a highly dislocation free (dislocation density $<10^5$ cm^{-2}) compound semiconductor epilayer on the substrate.

[0021] In another aspect, the present invention provides a semiconductor structure comprising a semiconductor substrate; a polycrystalline buffer layer on the substrate; an amorphous layer at an interface of the substrate and the buffer layer; and an epilayer of monocrystalline compound semiconductor on the buffer layer. The epilayer generally includes a monocrystalline template layer of the compound semiconductor grown on the buffer layer. Advantageously, the epilayer may comprise a compound semiconductor based device structure. In a preferred embodiment, the amorphous layer comprises an amorphous oxide layer, the buffer layer and epilayer are homoepitaxial or closely lattice matched and/or comprise the same material, and the compound semiconductor may comprise $Al_xIn_yGa_{1-x-y}N$ ($0<x, y<1$).

[0022] In another aspect, a semiconductor structure of the present invention may comprise a semiconductor substrate; a polycrystalline buffer layer on the substrate; an amorphous layer at an interface of the substrate and a buffer layer; and a monocrystalline template layer of compound semiconductor on the buffer layer. In a preferred embodiment, the amorphous layer comprises an amorphous oxide layer, the buffer layer and template layer are homoepitaxial or closely lattice matched and/or comprise the same material, and the compound semiconductor comprises $Al_xIn_yGa_{1-x-y}N$ ($0<x, y<1$) with a dislocation density $<10^5$ cm^{-2}.

Brief Description of the Drawings

[0023] Further aspects, features and advantages of the present invention will be readily apparent from the following detailed description, when read in conjunction with the accompanying drawings, in which:

[0024] FIG. 1 depicts a prior art semiconductor structure of an epilayer with high dislocation density on a substrate;

[0025] FIG. 2 illustrates a prior art semiconductor structure having an epilayer on a compliant universal substrate;

[0026] FIG. 3 depicts the deposition of a polycrystalline buffer layer on a substrate, in accordance with the principles of the present invention;

[0027] FIG. 4 depicts the creation of an amorphous layer at the interface between the buffer layer and substrate, by ion implantation through the buffer layer;

[0028] FIG. 5 depicts an alternative approach for creating an amorphous layer at the interface between the buffer layer and the substrate, by back-side ion implantation through the substrate;

[0029] FIG. 6. depicts the growth of a template layer on the buffer layer, according to the method of the present invention;

[0030] FIG. 7 schematically illustrates the formation of the highly dislocation free epilayer of the present invention; and

[0031] FIG. 8 shows the formation of a compound semiconductor based device structure in the epilayer.

Detailed Description

[0032] The present invention is generally directed to a method for forming or fabricating a highly dislocation free compound semiconductor on a lattice mismatched

substrate. In this method, a polycrystalline buffer layer is first deposited on the substrate, and then an amorphous layer is created at the interface between the substrate and the buffer layer, preferably by ion implantation. The resulting "floating" buffer layer serves as a seed layer for the growth of a high quality monocrystalline template layer and highly dislocation free compound semiconductor epilayer thereon.

[0033] By way of example, application of the method of the present invention to the formation of a highly dislocation free $Al_xIn_yGa_{1-x-y}N$ ($0<x, y<1$) based device structure on an exemplary silicon substrate, will now be described.

[0034] As shown in FIG. 3, a thin buffer layer 22 (e.g. 20 to 50 nm) of polycrystalline $Al_xIn_yGa_{1-x-y}N$ ($0<x, y<1$) is deposited on a silicon (Si) substrate 24 at a low temperature (e.g. 500°C using a MOCVD system) in a deposition system (not shown) such as metalorganic chemical vapor deposition (MOCVD) reactor or by molecular beam epitaxy (MBE). The purpose of buffer layer 22 is two fold. First, it serves as the seeding layer for the subsequent growth of a monocrystalline, high-temperature $Al_xIn_yGa_{1-x-y}N$ epitaxial layer (e.g. a thickness of higher than 500 nm), with high lattice matching between a monocrystalline template layer and the seeding layer. Secondly, it is compatible with oxygen ion implantation, i.e. its crystalline properties are not significantly changed by such ion implantation.

[0035] The sample 26 is then removed from the deposition system and an amorphous oxide layer SiO_x 28 is formed at the interface of the buffer layer 22 and the Si substrate 24 (i.e. with no Si overlayer above the oxide layer). The known Separation-by-IMplanted-Oxygen (SIMOX) method may be used for the formation of the amorphous oxide layer. The oxygen ion dose should be kept below the limit of amorphization of AlInGaN (about $8x10^{15}$ cm^{-2}). It is also preferable that the implantation be performed at elevated temperatures (e.g. several hundred degrees Celsius) for lowering any damage to the AlInGaN buffer layer 22 due to high energy ion implantation. The elevated temperature of ion implantation should be kept below the critical re-crystallization temperature of the amorphous oxide layer (i.e. below 800°C).

[0036] The ion implantation of the interface layer can be performed from either the top (through the buffer layer 22 as shown in FIG. 4) or bottom side (through the substrate 24 as shown in FIG. 5).

[0037] By oxygen ion implantation, the amorphous layer 28 is created that mechanically separates the lattice mismatched substrate 24 from the polycrystalline buffer layer 22 enabling a "floating" buffer layer for subsequent growth of a monocrystalline AlInGaN template layer, free from stress and dislocations and preferably lattice matched to the buffer layer.

[0038] Since polycrystalline materials are more flexible for structural arrangements, the polycrystalline AlGaInN buffer layer will only suffer minor damage by ion implantation, if implanted from the buffer layer side (top side) and can be easily cured through thermal annealing. Moreover, the ion beam irradiation in the present invention might even be beneficial for the buffer layer in the sense that the beam may reshape the size of the grains of the polycrystalline AlGaInN buffer layer to make them more uniform which will enhance the uniformity of the following epitaxial growth of an AlInGaN monocrystalline template layer.

[0039] In the variation shown in FIG. 5, the oxygen ion implantation can be done from the substrate side, preferably after thinning the substrate to less than 200 micron. This method is advantageous because of the its lower impact on causing possible damage to the polycrystalline buffer layer 28. In the back-side implantation, there will be no limit on the dose of the oxygen for implantation, which will lead to better and more continuous SiO_2 layer at the interface of the AlGaInN buffer layer 22 and the Si substrate 24, thus better mechanical isolation between them.

[0040] The sample (buffer layer 22 on amorphous oxide layer 28 on Si substrate 24) is then loaded into the deposition system for regrowth. As shown in FIG. 6, a highly dislocation free template layer 30, preferably lattice matched to the polycrystalline buffer layer 22, of monocrystalline $Al_xIn_yGa_{1-x-y}N$ with a thickness of about 1-3μm is then grown on the "floating" $Al_xIn_yGa_{1-x-y}N$ (seeding) buffer layer 22. This highly dislocation free

$Al_xIn_yGa_{1-x-y}N$ layer 30 will in turn be used as the template layer for the subsequent growth of a highly dislocation free epilayer 32 of $Al_xIn_yGa_{1-x-y}N$ (see FIG. 7), and Al_x-$In_yGa_{1-x-y}N$ -based device structures (see FIG. 8).

[0041] The device structures that can be potentially grown on the template layer include light emitters (light emitting diode and laser diode), photo detectors and sensors, solar cells matching the solar spectrum, high power and high frequency electronic devices, transistors, and quantum effect and high speed devices.

[0042] A general structure for a photo detector and light emitting diode or laser diode structure is schematically shown in FIG. 8 and includes a n-type layer 36, a p-type layer 38 sandwiching an active (e.g. undoped) region 40. The device structure may, of course, take different forms.

[0043] To develop high nuclei density of polycrystalline $Al_xIn_yGa_{1-x-y}N$ buffer layer on Si substrate, it is desirable, during the growth of AlInGaN on Si, to prevent formation of SiN_x on Si. Formation of SiN_x takes place due to competition between interaction of the Si substrate with nitrogen and formation of GaN on Si. The prevention of formation of SiN_x is important because the presence of SiN_x on Si will prevent formation of GaN layers on Si.

[0044] To this end, polycrystalline AlN has been deposited on a silicon substrate at a temperature of about 1000° C and growth initiation using six seconds of trimethy aluminum (TMAl) pulse in a MOCVD system, to form the thin polycrystalline buffer layer. The amorphous layer may be formed by nitrogen ion implantation, e.g. 50keV of nitrogen ions with a dose density of about $2x10^{16}cm^{-2}$ at temperatures of 200° C to 300° C. A thin dielectric mask on the AlN buffer layer may be used to prevent or reduce damage from implantation.

[0045] Accordingly, the method of the present invention facilitates monolithic integration of III-V devices on Si. This is highly desirable because Si is an excellent substrate material for III-V optoelectronic devices because of its good mechanical and

thermal properties, low cost and the availability of high quality wafers, currently with size up to 12-inch.

[0046] The substrate used in the present invention can be silicon, SOI, $Al_xGa_{1-x}As$ (where $x>0$), or any other substrate material that can be made to have an amorphous layer at its interface, e.g. by ion implantation. The buffer layer deposition conditions can be any appropriate conditions that create the desired polycrystalline buffer layer. The type of ions used in the ion implantation can be oxygen ions or other ions, such as, for example, nitrogen or silicon ions, that can be implanted into the substrate to create an amorphous layer at the interface between the buffer layer and the substrate. The buffer layer of the present invention should be compatible (lattice constant and thermal expansion coefficient) with the template layer to be epitaxially grown on it. Preferably, the buffer and template layers comprise materials with closely matched lattice constants and thermal expansion coefficients, in order to minimize the generation of dislocations. The material for the buffer and template layers can be from III-V compounds (including III-V nitrides), II-VI compounds, IV-VI compounds, Si_xGe_{1-x} ($0<x<1$) and other types of materials that semiconductor devices can be made from. Similarly the devices formed in the epilayer of the present invention can take a wide variety of forms.